IMPLEMENTATION OF QPSK ON FPGA USING LUT

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ABSTRACT: *Modulation is the process of translation of a source signal to a signal with improved frequency. Modern Communication systems use digital modulation techniques because of having advantages like greater noise immunity and robustness to channel impairments. It does offer more flexibility as well as greater security. One of the digital modulation techniques that are capable to maintain a low Bit Error Rate (BER) even if the received signal strength is extremely low is Quadrature Phase Shift Keying (QPSK). Implementing QPSK on a Hardware Descriptive Language, HDL instead of Board Processing Systems like PCB is the main motive of this paper. The paper is based on design and implementation of a QPSK Modulator on FPGA. The simulation was made in Verilog, HDL (a tool used for FPGA Designing. By attempting this majority of the limitations primarily cost and design size can be resolved.*

KEYWORDS: QPSK (Quadrature Phase Shift Keying), FPGA (Field Programmable Gated Array), HDL (Hardware Descriptive Language), BER (Bit Error Rate), PCB (Printed Circuit Board), LUT (Look UP Table), PSK (Phase Shift Keying), BPSK (Binary Phase Shift Keying), FM (Frequency Modulation)

INTRODUCTION:

QPSK is a phase modulation algorithm that is a version of FM, Frequency Modulation. In Phase Modulation the carrier frequency is modulated to encode the digital information in bits in each phase change. The term "PSK" refers to Phase Shift Keying in QPSK. It is a phase modulation technique in which discrete number of states is accomplished. QPSK has four states. Half number of states is known as "Binary Phase Shift Keying" (BPSK).

Dobkin (2005) explained, that any digital modulation technique used would have a finite number of distinct signals to represent the digital data. In PSK a finite number of phases are used [1]. Each phase used is assigned with a unique pattern of bits in binary. Mostly equal number of bits is encoded by each phase. The symbol is formed by each bit patterns, represented by a particular phase.

In QPSK two sinusoids (Sine and Cosine) are the fundamental functions for Modulation. The Modulation is achieved by the phase variations of the fundamental functions that depend on the actual message symbol. Each symbol in QPSK contains two bits. The mathematical equation that represents QPSK is:

$$s_i(t) = \sqrt{\frac{2E_s}{T}} cos(2\pi f_c t + (2n-1)\frac{\pi}{4}) \quad \text{,n=1,2,3,4} \tag{1}$$

In the above equation n=1, having the phase sift of 45 degrees. This very type is also known as pi/4 QPSK. If the constellation diagram of QPSK is drawn it will reflect that the constellation points lie on the 'x' and 'y' axis. It means that the QPSK will have one in-phase component and one quadrature component. The former is represented by (I) and the later by (Q).

MAJOR ADVANTAGES OF QPSK:

Verdu (2002) explained that QPSK offers power and spectral efficiency [7]. Because of this reason it is used in communication channels in satellite communication systems. Bandwidth optimization is the most important aspect of Modulation. Better bandwidth efficiency is provided by QPSK. The ratio of data rate to channel bandwidth is called bandwidth efficiency. It is measured in (b/s/Hz). When the (I) and (Q) signals are same, QPSK results in the optimum use of both the spectrum and the power.

Considering PER, Probability of bit error calculation it is same as for BPSK. Stallings (2009) and Stuber (2011) explained that the similarity between Binary Phase Shift Keying, BPSK and Quadrature Phase Shift Keying, QPSK is that both the modulation schemes do hold the same probability of bit error [5][6]; which is;

$$P_b = Q\left(\sqrt{\frac{2E_b}{N_0}}\right). \tag{2}$$

To achieve the same bit error of BPSK, twice power is utilized because in QPSK two bits are transmitted simultaneously. Stuber (2011) explained that the Symbol rate is given by the expressions [6]:

$$P_s = 1-(1-P_b)^2$$
$$= 2Q\left(\sqrt{\frac{E_s}{N_0}}\right) - Q^2\left(\sqrt{\frac{E_s}{N_0}}\right) \tag{3 \&4}$$

Considering the SNR, Signal to Noise Ratio is high that is a fundamental aspect of QPSK systems, the symbol error probability is approximated.

$$P_s \approx 2Q\left(\sqrt{\frac{E_s}{N_0}}\right) \tag{5}$$

In practice the differential encoded QPSK is mostly used because the BPSK offers ambiguity problems at the destination/ receiver end.

IMPLEMENTATION OF QPSK:

As explained in the introduction section that sine and cosine are the fundamental variables of QPSK Modulation that is given by;

$$s_i(t) = \sqrt{\frac{2E_s}{T}} cos(2\pi f_c t + (2n-1)\frac{\pi}{4}) \quad \text{,n=1,2,3,4} \tag{6}$$

That reflects to the fact that four phases are needed, Pi/4, 3Pi/4, 5Pi/4 and 7Pi/4. Two signal space with unit base functions are resulted from the above expression. The first

expression yields for the (I) component and the second one is for (Q)

$$\phi_1(t) = \sqrt{\frac{2}{T_s}}\cos(2\pi f_c t)$$

$$\phi_2(t) = \sqrt{\frac{2}{T_s}}\sin(2\pi f_c t) \quad (7 \& 8)$$

Hence the constellation diagram consists of four signal-space points.

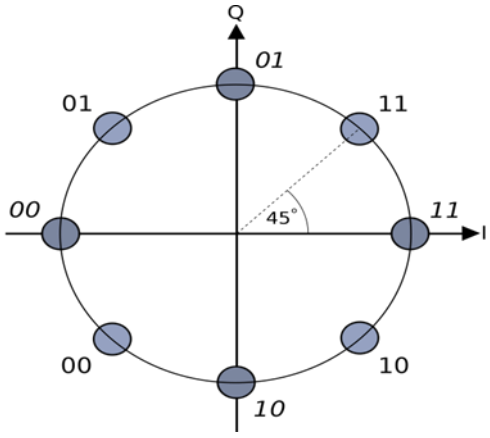

Figure 01: Constellation Diagram of QPSK [5]

Table 01: Constellation Table of QPSK

I stream	Q stream	Result
0	0	Cos (wt + 45)
0	1	Cos (wt + 135)
1	0	Cos (wt - 45)
1	1	Cos (wt - 135)

SIFNIFICANCE OF FPGA AND HARDWARE DESCRIPTIVE LANGUAGE:

FPGA, Field Programmable Gated Array Technology does very much work on the MOORE's Law. Statistics shows that there is a phenomenal growth in FPGA technology. Sagdeo (1998) stated that the first Hardware Descriptive Language, HDL that was designed to not only model the Digital System but also to simulate, synthesize, analyze and test the design is Verilog, HDL. Moreover it handles the complexity of the design accurately and precisely [4].

Sagdeo (1998) mentioned that in 1995, Verilog, HDL was standardized by IEEE. Moreover this language is not only used to simulate but also to synthesize a highly complex Digital System Design [4]. Padmanbhan and Sundari (2003) explained that designing in Verilog, HDL is very similar to C-programming [2].

The benefits that FPGA provides are:

- "Glue Logic" is considered to be the most essential prospect ass every system needs it. It provides support to connect large Integrated Circuits (IC's).
- FPGA does offer performance improvisation. If FPGA is considered against Microprocessors it offers circuit customization by Yiannacouras (2009) [8].
- Because of Hardware Descriptive Language, system complexity is reduces as well as the manufacturing cost is reduced.
- Often in the electronics and communication industry IC's are relatively very expensive to develop.
- FPGA's are reconfigurable that offers flexibility in the design.

Because of the above-mentioned reasons, instead of implementing QPSK on printed board technologies an attempt is made to switch the design on HDL and FPGA Technology [9].

IMPLEMENTATION OF QPSK ON VERILOG HDL

Because of the Digital nature of Verilog HDL it apparently appears impossible to generate Analog Signals. False because methods can be developed to tackle this. The method used in this implementation is a "Look UP Table" (LUT). In Computer Sciences, a LUT is defined as a data structure, usually an array or an associative array, being used to replace a run time computation with a simpler array indexing operation. The speed gain can be significant as retrieving memory is comparable faster to expensive computation.

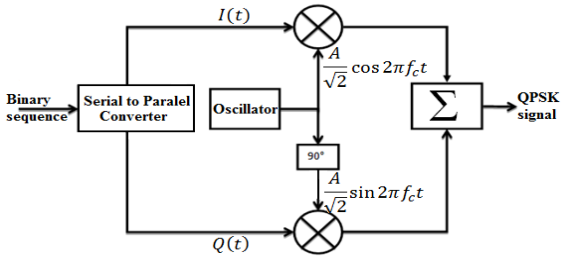

Figure 02: Block Diagram of a QPSK Modulator [5]

LUT was developed in this implementation. The samples of a sine wave are stored in a table and these samples are picked according to the required frequency of wave. For the slowest frequency every value of the table is read. To achieve higher speed some vales are skipped.

In this proposed design a LUT with 100 locations are designed. Or it is said that the LUT has 100 sample values. Sine wave is started from Location 0 as it starts from 0 degrees and to cosine wave is started from the location no 24 as it has a phase shift of 90 degrees.

Below is the algorithm that was adopted to design a QPSK Modulator.

DESIGN AND IMPLEMENTATION OF LUT:

In this very implementation, first of all a Sine Wave was drawn manually. Then Sine wave was sampled manually. After doing that the values are marked on the sine waves.

On the basis of the manual representation of the Sine wave, the samples were stored in a Look UP Table. These samples are selected on the basis of the required frequency of the Sine and cosine waves.

- Digital Data can either consist of 0 or 1 Data Bits
- If Data transmitted to the I Stream is 0, NO Phase Shift in the Sine Wave
- If Data transmitted to the I Stream is 1, The Sine Wave will introduce a Phase Shift
- If Data transmitted to the Q Stream is 0, NO Phase Shift in the Cosine Wave
- If Data transmitted to the Q Stream is 1, The Cosine Wave will introduce a Phase Shift

Table 02: Look UP Table

Location No.	Location Value
Location 0	100
Location 1	105
Location 2	110
Location 3	120
Location 4	130
Location 5	135
Location 6	140
Location 7	150
Location 8	160
Location 9	170
Location 10	180
Location 11	190
Location 12	200
Location 13	190
Location 14	180
Location 15	170
Location 16	160
Location 17	150
Location 18	140
Location 19	135
Location 20	130
Location 21	120
Location 22	110
Location 23	105
Location 24	100
Location 25	95
Location 26	90
Location 27	80
Location 28	70
Location 29	65
Location 30	60
Location 31	50
Location 32	40
Location 33	30
Location 34	20
Location 35	10
Location 36	5
Location 37	1
Location 38	5
Location 39	10
Location 40	20
Location 41	30
Location 42	40
Location 43	50
Location 44	60
Location 45	65
Location 46	70
Location 47	80
Location 48	90
Location 49	95

One Look UP Table is used for the Generation of Both Sine and Cosine Waves. As Sine Waves Starts from Location 0 so an Index is set to be on the 0^{th} Location and for Cosine Wave the Index is set on the Location 12^{th}. Repeated, sine and cosine waves can be generated by resetting the Index Value. Also because of the fact that Verilog, HDL does not support the negative values so a threshold can be set which is the value of 95 in the LUT, Look UP Table.

As the Total Number of Locations are 50 starting from 0 to 49 covering from 0 to 360 Degrees, it means that in order to introduce the Phase Shift of 180 Degrees in the Sine and Cosine Wave, Location 24^{th} has to be used.

The Algorithm is implemented by:

Sine Wave is Multiplied by I Stream; If I= 0, NO Phase Shift, If I = 1 Phase Shift = 180 Degree.

Cosine Wave is Multiplied by I Stream; If I= 0, NO Phase Shift, If I = 1 Phase Shift = 180 Degree.

Output = Summation of both the waves; Total Bits =9

RESULTS:

The theoretical wave that should be achieved for QPSK given by Popescu, Gonteanand and Ianchis in (2011) [3] are:

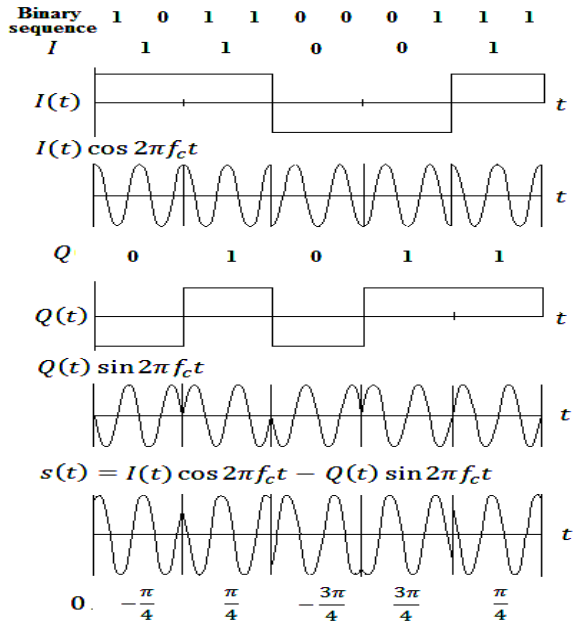

Figure 03: Theoretical wave form of QPSK Modulator

The final result achieved after the implementation of QPSK in Verilog HDL is given in the figure below:

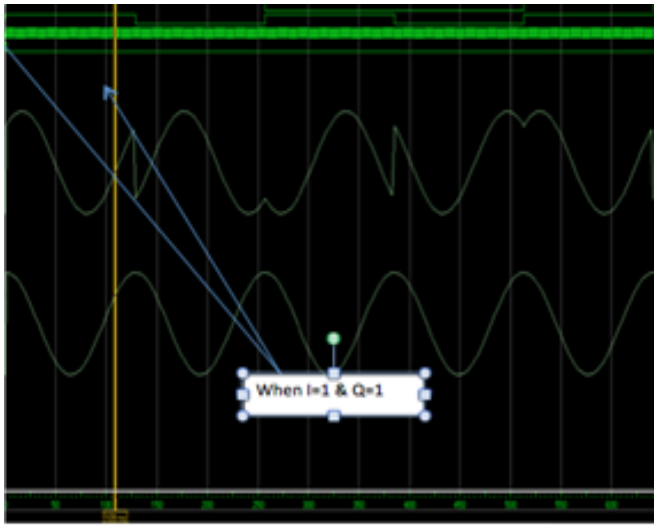

Figure 04: Justification of QPSK Modulator with (I) and (Q) bit streams.

CONCLUSION:

The paper presents the implementation and design of a QPSK Modulator on Verilog HDL to be used on FPGA. The methodology used is Look UP Table.

By using Verilog HDL not only the hardware design of QPSK Modulator was achieved but also a new dimension to the communication system designers is given that a cost effective solution can be provided, by using this power FPGA Technology.

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